Push Button Telephone Dialers

FEATURES: AY-5-9151A

- 2.5V to 5V and 200μA operation, plus standby mode
- Frequency of on-chip clock set by external RC network
- Selectable break: make ratio and interdigital pause
- Uses 3 x 4 matrix keyboard with no keyboard ground or common contact
- Keyboard inputs have antibounce protection
- Input pull-up or pull-down resistors on-chip
- Redial and access pause controlled from keyboard
- 22 digit capacity including access pauses
- Dialer reset for line power breaks >200ms.

FEATURES: AY-5-9151B. Same as AY-5-9151A except:

- 18 Pin package

FEATURES: AY-5-9152. Same as AY-5-9151A except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

FEATURES: AY-5-9152/B. Same as AY-5-9152 except:

- 18 Pin package

FEATURES: AY-5-9153A. Same as AY-5-9151A when in 3 x 4 matrix keyboard mode plus:

- Pin selectable options of 1 of 12 keyboard, 2 of 7 keyboard wired to produce 4-bit code with common
- 8 bit output for displaying number in digit store
- Simple call-barring facility using display outputs

FEATURES: AY-5-9153B. Same as AY-5-9153A except:

- Keyboard is binary input with common

FEATURES: AY-5-9154A. Same as AY-5-9153A except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

DESCRIPTION

This range of CMOS Pushbutton Dialers consists of seven devices AY-5-9151A to AY-5-9154A, all of which perform the function of converting input data (e.g. from a keyboard) into a series of pulses suitable for loop disconnect dialing. The series is based on two devices: a simple, basic dialer circuit and a more complex and versatile device which accepts a variety of data entry codes and has a display facility.

The use of CMOS technology results in low voltage and current requirements, enabling easy interfacing with a variety of telephones. The versatility of the devices and the low external component count enables the building of sophisticated, reliable telephones at low cost.

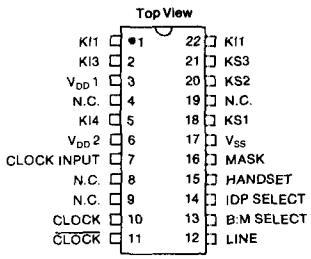
Part Number	Min Supply Voltage	# of Pins	IDP Pin Select	B:M Pin Select	# of Positive Voltage Supply Pins	Keyboard	Two Antiphase Mask Outputs	Display Capability
*AY-5-9151A	2.5V	22	700, 800 500ms	yes	2	4 x 3	no	no
*AY-5-9151B	2.5V	18	700, 800 500ms	yes	2	4 x 3	no	no
*AY-5-9152	2.5V	22	700, 800 500ms	fixed (60:40)	2	4 x 3	yes	no
*AY-5-9152/B	2.5V	18	700, 800 500ms	fixed (60:40)	2	4 x 3	yes	no
*AY-5-9153A	2.5V	28	700, 800 500ms	yes	2	4 x 3 1 of 12 4 bit & common	no	yes
*AY-5-9153B	2.5V	28	700, 800 500ms	yes	2	binary input	no	yes
*AY-5-9154A	2.5V	28	700, 800 500ms	fixed (60:40)	2	4 x 3 1 of 12 4 bit & common	yes	yes
*AY-5-9158	2.5V	18	800, 500ms	fixed (66.7:33.3)	1	4 x 3	no	no

*Redial capability: 22 digits
Dial Rate: 10pps

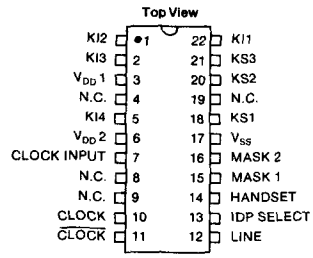
PIN CONFIGURATIONS

22 LEAD DUAL IN LINE

AY-5-9151A



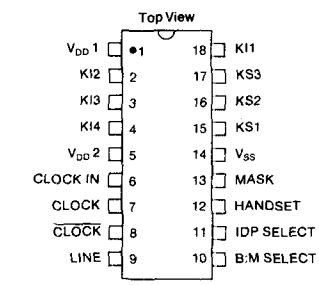
AY-5-9152



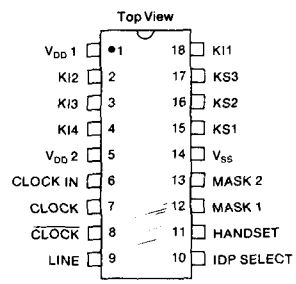
PIN CONFIGURATIONS

18 LEAD DUAL IN LINE

AY-5-9151B



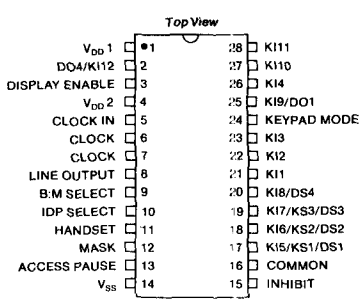
AY-5-9152B



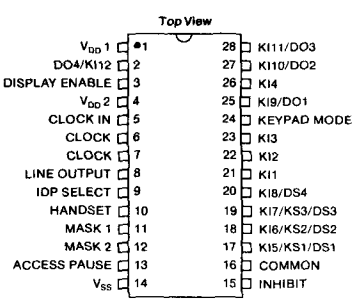
PIN CONFIGURATIONS

28 LEAD DUAL IN LINE

AY-5-9153A/9153B



AY-5-9154A



PIN FUNCTIONS

V_{SS} - The negative supply to the device. All voltages are referenced to this pin.

V_{DD1} - The positive supply to the digit store and write counter. Power must be maintained on this pin if the redial function is used.

V_{DD2} - The positive supply to the clock generator and control logic. V_{DD2} should rise to 2.5V within 20ms of switch-on.

Clock In, $\overline{\text{Clock}}$, Clock - These pins are connected to an external RC network which controls the frequency of the clock generator and hence the timing of the line and mask outputs.

Handset Input - The state of the handset is used to control this input, a logic 1 on the input indicating that the handset is on-hook and a logic 0 indicating that the handset is off-hook. This input is used to reset the control logic depending on the past history of the input.

If the input is taken from logic 1 to logic 0, and the clock is not oscillating, a reset pulse is produced when clock pulses are detected. The device is then ready for operation.

If the input is taken to logic 1 for less than 200ms and the clock generator is operating throughout this period, a reset pulse is not produced when the input is taken back to logic 0. Thus short breaks in line power will not affect the operation of the circuit.

If the input is taken to logic 1 for more than 200ms, and clock pulses are present throughout this period, a reset pulse will be generated at the end of the 200ms period.

Line Output - The loop disconnect dial pulses appear at this output. It is an open drain output with the source of the output transistor being connected to V_{SS}. A break period corresponds to this transistor being switched on and a make period or IDP corresponds to the transistor being switched off. The first digit of any outdialing sequence is preceded by a pre-digit pause equal in length to an interdigital pause.

Mask Output/Mask 1 Output - This is a push-pull output and is used to mute the telephone speech circuit. A logic 1 indicates that the speech circuit is to be muted, this occurring immediately on recognition of an input from the keypad.

Mask 2 Output — The AY-5-9152/B and AY-5-9154A are fixed at 60:40 Break:Make ratio and a Mask 2 output is substituted for the Break: Make input. The mask 2 output is identical to the mask 1 but is driven in antiphase to enable a bistable mask relay to be used.

On initial application of power, a pulse is produced on Mask 1 and Mask 2 outputs to reset a bistable relay which may be connected to these outputs.

IDP Input - This pin is used to select the duration of the interdigital pause. With a clock frequency of 18kHz, interdigital pauses of 700, 800 or 500ms may be selected.

Break: Make Ratio — A choice of four break:make ratio is available as a pin programmable option, 70:30, 66.6:33.3, 60:40 and 50:50.

Display Enable - When display data is being output from the dialer, this output goes to a logic 1.

Common Input - When a 4 bit code is used for data input a logic 1 on this input strobes the data into the device. Antibounce protection is provided for this input. A steady logic 1 of less than 5ms duration will not be recognized and a steady logic 1 of greater than 10ms duration will be recognized. This input has a pull down resistor to V_{SS}.

Inhibit Input - This is used to inhibit outdialing. If a logic 1 is placed on this input while a digit is being dialed, outdialing will cease when the digit has been completed. If the logic 1 appears during an IDP, outdialing will cease immediately. When outdialing has ceased, the Mask 1 output goes to logic 0 and Mask 2 goes to logic 1. When the input is taken to logic 0, the Mask signal reappears and dialing continues, starting with an IDP.

Access Pause Output - When an access pause is reached in the dialing sequence, this output goes to logic 1. By connecting this to the inhibit input, further outdialing will be prevented.

Keyboard Mode - The data on this pin determines whether the device will accept data from:

a) 1 of 12 keyboard with keyboard ground
b) 2 of 7 keyboard with keyboard ground and common switch
c) 4 bit binary code with common signal
d) 4 x 3 matrix keyboard without keyboard ground and common switch

When modes b, c or d are in use with the AY-5-9153A/B or AY-5-9154A data in the form of two, four-bit words is available for display purposes, except when a key is pressed.

Keyboard Inputs/Keyboard Scans/Display Outputs 1 of 12 Mode - All twelve pins are used as keyboard inputs, on-chip pull-up resistors to logic 1 being incorporated. A logical AND of the twelve inputs produces an on-chip Any Key Down signal when any input is taken to logic 0. Detection of this signal initiates an anti-bounce period and at the end of this period, the data on the twelve inputs is read into the digit store, provided the Any Key Down signal is present throughout this period. Any further data is then inhibited until an antibounce period has been completed with all keys up. If, during the anti-bounce period, the Any Key Down signal disappears, the anti-bounce timer will be reset.

2 of 7 Mode - Keyboard inputs 1-4 are used for the 4-bit data, the common input strobing the data into the digit store. On-chip pull down resistors to logic 0 are incorporated on the four data inputs and the common input. When the common input is taken to logic 1, an antibounce timer is started and if the common input is at logic 1 throughout, the data is read at the end of the period. Further data is then inhibited until the common input has been at logic 0 for an antibounce period.

Binary Mode - The 4-bit word is entered into the digit store via inputs 1-4 by use of the common input, in a similar manner to the 2 of 7 mode. On-chip pull down resistors to logic 0 are incorporated. When data is not being read into the device (i.e. when the common input is at logic 0) these four inputs are used as output pins for a 4-bit word for digit display purposes as described later.

4 x 3 Matrix Mode — This function will be described for the AY-5-9151 Series, and AY-5-9152/B. The mode of operation is slightly different for the AY-5-9153A/B and AY-5-9154A, as explained later.

A pulse to logic 0 is sequentially switched around the three keyboard scan outputs, taking 5ms for a complete scan cycle. When a key is pressed the pulse appears on one of the four keyboard inputs 1-4 (provided with pull-up resistors to logic 1), and if it occurs on the same input on the next scan cycle, the data is entered into the digit store. Before a second key depression may be recognized, the first key must be released and a full scan cycle completed without a pulse on any input.

If two keys are pressed during the same scan cycle, the data will be rejected and again a full scan cycle must be completed without a pulse appearing on any of the inputs before another key depression may be recognized.

If a key is pressed during an inhibit period, or two keys are pressed simultaneously, all three scan outputs will go to logic 0 until the key or keys is/are released.

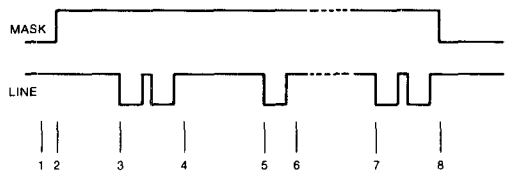
Display Scans/Display Outputs - Data for the first 16 digits and access pauses in the store is available for display.

The position of a digit within a telephone number is indicated by a 4 bit binary word from the Display Scan outputs. Display Scan 1 is the least significant bit and Display Scan 4 is the most significant bit. Binary word 0000 corresponds to the left-hand digit of the display (the first number entered) and 1111 corresponds to the right-hand (16th) digit of the display.

The digit being output is available as a 4 bit word on the display outputs (Display Out 1 = least significant bit). Binary word 0001 represents digit 1 and so on to 0000 = digit 10. Access pauses are represented by 1011.

When in the 2 of 7 mode or the Binary mode, the display data is inhibited by the appearance of the common signal. When in the 4 × 3 matrix mode, depression of a key causes display scan data to appear on the keyboard inputs. The dialer then reverts to the normal keyboard scanning mode of operation.

LINE AND MASK OUTPUT TIMING



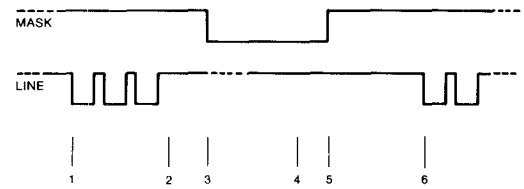
The above sequence of events is that which occurs when the digit store is initially empty. The time intervals quoted in the following explanation are valid only for a clock frequency of 18kHz. The time intervals are inversely proportional to the clock frequency.

	Event	Time Interval
1	The first key is depressed and the anti-bounce timer is started	T_{1-2} = 5-10ms after end of bounce
2	The data from the keyboard is accepted. The mask output appears and the pre-digital pause commences. This is the same duration as the inter-digital pause and is pin selectable.	T_{2-3} = 700, 800, or 500ms
3	Dialing of the first digit starts. The example shown is a digit 2.	T_{3-4} = n × 100ms where n = digit dialed
4	End of 1st digit and start of inter-digital pause.	T_{4-5} = 700, 800, or 500ms
5	Dialing of 2nd digit starts. The example shown is a digit 1.	T_{5-6} = n × 100ms where n = digit dialed
6	End of 2nd digit and start of inter-digital pause.	T_{6-7} = 700, 800, or 500ms

Dialing of further digits continues in a similar manner until the last digit.

7	Dialing of last digit commences, in this case a digit 2.	T_{7-8} = n × 100ms where n = digit dialed
8	End of last digit and end of mask signal.	

EFFECT OF ACCESS PAUSE ON LINE AND MASK OUTPUT TIMINGS



The following time intervals are valid only for a clock frequency of 18kHz.

	Event	Time Interval
1	Dialing of the last digit before the access pause commences. A digit 3 is shown in this example.	T_{1-2} = n × 100ms where n = digit dialed.
2	The end of the last digit before the access pause.	T_{2-3} = 700, 800, or 500ms
3	The mask signal is removed so that the telephone user can listen for the appearance of the second dial tone.	
4	The telephone user presses the # key to release the access pause. The antibounce timer is started.	T_{4-5} = 5-10ms
5	The data from the # key is accepted or the inhibit input is taken to logic 0 and the mask signal reappears. A pre-digital pause equal in length to an inter-digital pause starts.	T_{5-6} = 700, 800, or 500ms
6	The digit after the access pause is dialed out. Dialing then continues as normal.	

Access Pause and Redial Operation

These facilities are available on all devices, control being via the keypad or data input codes. The 1 of 12 keypad and 4 × 3 keypad use the '*' button to insert an access pause and the '#' button to release the access pause.

The '#' button may also be used to redial the number in the digit store. If the redial mode is used, power must be maintained on V_{DD1} at all times.

PIN SELECTABLE OPTIONS

a) Break:Make Ratio

Ratio	Voltage On Pin
70:30	Clock
66.6:33.3	V_{DD}
60:40	V_{SS}
50:50	Clock

b) IDP (with 18kHz clock frequency)

IDP	Voltage on Pin
700ms	V_{DD} 2
800ms	V_{SS}
500ms	Clock

c) Keyboard Mode

Mode	Voltage On Pin
2 of 7	V_{DD}
3 × 4	V_{SS}
1 of 12	Clock
Binary	Clock

DATA INPUT CODES

KI = Keyboard Input

Binary

KI 4	KI 3	KI 2	KI 1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	Access Pause
1	1	0	0	Redial

2 of 7

KI 1	KI 2	KI 3	KI 4	Digit
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	7
1	0	0	1	8
1	0	1	0	9
0	0	1	1	10
1	1	0	0	Access Pause
1	1	0	1	Redial

4-bit codes other than those shown above are ignored.

DATA OUTPUT CODES

Display Scan (DS)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DS4	DS3	DS2	DS1	Position
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

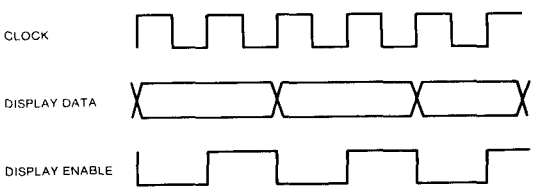
Display Outputs (DO)

DO4	DO3	DO2	DO1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	0
1	0	1	1	Access Pause

The Display Scan outputs are continuously incremented, and the Display outputs changed accordingly, to enable the display of all the digits in the digit store by the use of multiplexing.

The Display Scan code is incremented at half the clock frequency.

The relationship between Clock, Display Data out and Display enable is as follows.



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... +7.0V to −0.3V
Storage Temperature Range ..... −65°C to +150°C

Standard Conditions (unless otherwise noted):

$V_{SS} = 0V$
$V_{DD1} = V_{DD2} = 2.5V$ to 5.0V ($V_{DD1} \geq V_{DD2}$)
$T_A = -25°C$ to +85°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Clock frequency = 18kHz The device will function correctly from 8kHz to 50kHz but all timings (break period, IDP etc.,) will be directly dependent on the clock period.

Characteristic	Min.	Typ.	Max.	Units	Conditions
Inputs					
IDP, B:M, Key Pad Mode					
Logic '0' Level	−0.3	—	0.2	V	
Logic '1' Level	V_{DD2} −0.2	—	V_{DD2}+0.3	V	
All Other Inputs					
Logic '0' Level	−0.3	0	0.5	V	Note 1
Logic '1' Level	V_{DD2} −0.5	V_{DD}	V_{DD2} +0.3	V	
Capacitance	—	—	10	pF	$V_{IN} = V_{SS}$, f = 1MHz
CURRENT SOURCE TO V_{DD2}					
Keyboard Inputs	2	—	60	μA	
CURRENT SINK TO V_{SS}					
Keyboard Inputs Common IDP, B:M	3	—	90	μA	
	0.6	—	15	μA	
Clock In Leakage Current	—	—	20	nA	$T_A = +25°C$ $V_{IN} = V_{SS}$ or V_{DD1}
Key Depression Period	10	—	—	ms	
OUTPUTS					
LINE:					
Logic '0' Output Current	2	—	—	mA	$V_O = 1.0V$
Logic '1' Leakage Current	—	—	1	μA	$V_O = 5.0V$
MASK:					
Logic '0' Output Current	2	—	—	mA	$V_O = 1.0V$
Logic '1' Output Current	2	—	—	mA	$V_O = V_{DD2} - 1.0V$
ALL OTHER OUTPUTS:					
Logic '0' Output Current	0.1	—	—	mA	$V_O = 1.0V$
Logic '1' Output Current	0.1	—	—	mA	$V_O = V_{DD} - 1.0V$
CLOCK FREQUENCY	17.2	—	18.6	kHz	$V_{DD1} = V_{DD2} = 3.75V$
	14.3	—	—	kHz	$V_{DD1} = V_{DD2} = 2.5V$
	—	—	19.5	kHz	$V_{DD1} = V_{DD2} = 5.0V$
Temperature Stability	—	—	±2	%	Relative to value at +25°C $V_{DD2} = 5.0V$
	—	—	±5	%	Relative to value at +25°C $V_{DD2} = 2.5V$
SUPPLY CURRENT					
I_{DD1}	—	—	7	μA	$V_{DD1} = 5.0V$, $V_{DD2} = 0V$
I_{DD2}	—	—	200	μA	$V_{DD2} = 5.0V$, Note 2

NOTES:

1. The device will function correctly with a maximum logic '0' of 1.0V and a minimum logic '1' of V_{DD} −1.0V. However, use under these conditions may result in an increased supply current.
2. Measured with Break: Make, IDP, Inhibit and Keyboard Mode inputs at V_{SS}, and with no keys depressed.

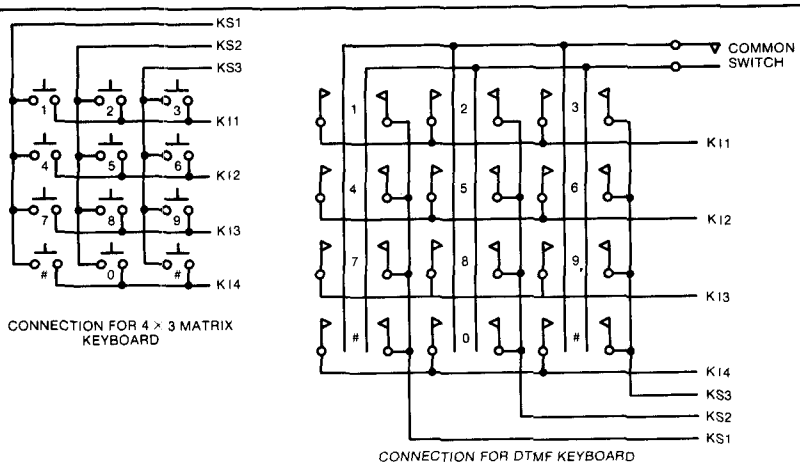


Fig. 1 KEYBOARD CONNECTIONS FOR AY-5-9151A & AY-5-9152

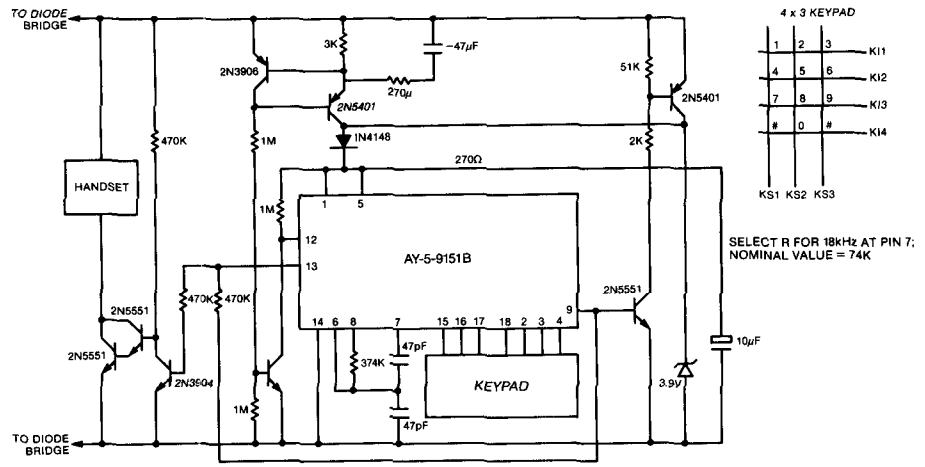


Fig. 2 PROVISIONAL PUSH-BUTTON DIALER CIRCUIT USING AY-5-9151A

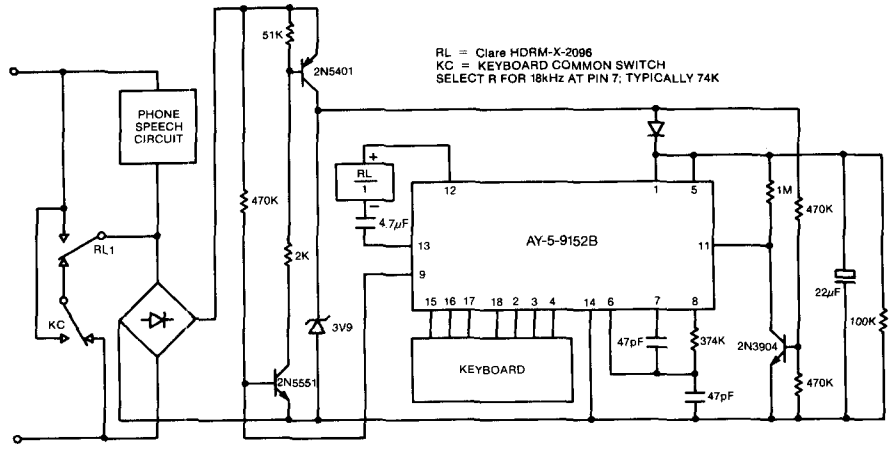


Fig. 3 PUSHBUTTON DIALER USING MASK RELAY